DOCKET NO. STMI07-02021 **PATENT**
CUSTOMER NO.: 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Franck Badets et al.
Serial No.:	10/603,579
Filed:	June 25, 2003
For:	VARIABLE PHASE-SHIFTING CIRCUIT, PHASE INTERPOLATOR INCORPORATING IT, AND DIGITAL FREQUENCY SYNTHESIZER INCORPORATING SUCH AN INTERPOLATOR
Group No.:	2816
Examiner:	Tuan Thieu Lam
Confirmation No.:	4869

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY BRIEF

Sir:

Appellants herewith respectfully submit that the Examiner's decision of August 5, 2008, rejecting Claims 1-2, 24-29 and 33-36 in the present application, should be reversed, in view of the following arguments and authorities. This Brief is submitted in response to the Examiner's Answer mailed April 14, 2009, and responds to the issues and arguments raised therein. No fee is believed due, but please charge any additional necessary fees to Deposit Account No. 50-0208.

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Real Party in Interest

The real party in interest, and assignee of this case, is STMicroelectronics, S.A.

Related Appeals or Interferences

To the best knowledge and belief of the undersigned attorney, there are none.

Status of Claims

Claims 1-2, 24-29 and 33-36 are under non-final rejection, and are each appealed. These claims were finally rejected on August 5, 2008, and an original Appeal Brief was filed on January 12, 2009.

Claims 3, 30-32 and 37-39 have been objected to.

Claims 4-23 have been withdrawn due to a restriction requirement.

Status of Amendments after Final

No amendments were made after final rejection, or after the most recent non-final rejection.

Summary of Claimed Subject Matter

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

A Summary of Claimed Subject Matter and Support for Independent Claims is found in the Appeal Brief, and is hereby incorporated by reference.

Grounds of Rejection to be Reviewed on Appeal

1. Are Claims 1-2, 24-29 and 33-36 anticipated by Dai, et al., (U.S. Patent 6,469,585, hereinafter "*Dai*")?

ARGUMENT

Stated Grounds of Rejection

The rejections outstanding against the Claims are as follows:

1. In the August 5, 2008 Office Action, Claims 1-2, 24-29 and 33-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dai, et al., (U.S. Patent No. 6,469,585, hereinafter "*Dai*").

Legal Standards

The relevant legal standards were discussed in the Appeal Brief, and are incorporated by reference.

Analysis of Examiner's Rejection

The discussion herein is addressed to the points raised in the Examiner's Answer. The arguments of the Appeal Brief are incorporated by reference.

First Ground of Rejection

Claims 1-2, 24-29 and 33-36 were rejected under 35 U.S.C. § 102(e) as being anticipated by Dai, et al., (U.S. Patent No. 6,469,585, hereinafter "*Dai*").

The Applicant's arguments discussed in the Appeal Brief filed January 12, 2009, with respect to this ground of rejection are incorporated herein by reference.

Claims 1-2, 24-29, and 33-36

These claims may be considered together.

Variable Phase-Shifting Circuit

In the Examiner's Answer, the Examiner essentially reproduces his argument made in the August 5, 2008 Office Action with respect to this element. The Examiner tries to offer some clarification regarding the functions of the elements of *Dai* he believes are applicable in teaching the variable phase-shifting circuit, as recited in Claims 1, 24 and 33. On Page 4 of the Examiner's Answer, the Examiner argues that Figure 3 of *Dai* is a "variable delay circuit with delay time [sic] is variably controlled by the control signal." Also on page 4, the Examiner argues that Figures 4 and 5 illustrate that the input and output signals are relatively phase shifted with one another. The Examiner concludes that "the limitation of a variable phase shifter circuit is fully met." However, other than specifically identifying a figure in *Dai*, the Examiner offers no new support for his argument that the delay stage (32) in *Dai* teaches a variable phase-shifted circuit, as recited in Claims 1, 24 and 33. The Applicant has clearly outlined on Pages 15-16 of the Appeal Brief that the delay

circuit (32) fails to teach a variable phase-shifter circuit. Furthermore, *Dai* expressly states:

> Delay stage 32 also includes **frequency tuning circuitry** including PMOS transistors M1 and M7 and NMOS transistors M4 and M10. PMOS transistors M1 and M7 each receive V_{CNTRL} at their gates, and function as variable resistors to **tune the amount of delay** of the delay stage 32, and hence the frequency of the VCO 30. (*Dai*, col. 4, lns. 23-28), (Emphasis added).

Clearly, *Dai* expressly teaches that only the frequency is tuned. *Dai* contains no teaching or suggestion that phase is tuned. Additionally, *Dai* teaches, and is limited to teaching, that each delay stage (32A and 32B) causes a fixed ninety degree phase shift. Therefore, *Dai* does not teach, expressly or inherently, a variable phase shifting circuit, as recited by independent Claims 1, 24 and 33.

Synchronized Oscillator

With respect to the element "a synchronized oscillator", on Pages 4 and 5 of the Examiner's Answer, the Examiner again essentially reproduces his argument made in the August 5, 2008 Office Action. The only new information the Examiner has added in his response is that M5 and M6 provide a feedback connection in which the output signal is feed to the input terminal thus "constituting a synchronized oscillator". The Examiner also notes that Appellant's own disclosure illustrates cross coupled transistors. Apparently, since the Examiner has identified cross coupled transistors in *Dai* and Appellant's disclosure, the Examiner concludes that "the limitation of a synchronized oscillator is met." However, other than identifying an alleged function of the control signal and the cross coupled transistor in Appellant's disclosure, the Examiner has not offered any additional support for his position, the Applicant reiterates what has clearly been outlined on Pages

16-17 of the Appeal Brief: Selecting a target a target control register does not teach enabling a target control address.

Regarding the Examiner's contention that M5 and M6 provide feedback which constitutes the "synchronized oscillator", the Examiner further argues that the auxiliary clock ht of Heberle is a recovered clock pulse. On Page 22 of the Examiner's Answer, the Examiner states that "the control signal (VCNTRL) in combination with the input signal changes the switching state inside the loop, hence controlling the free running oscillator." However, *Dai* actually states that the memory element 35 (comprised of M5 and M6) remains constant and operates to prevent the outputs of inverters 33 and 34 from switching states when the otherwise would switch. (*Dai*, col. 5, ln. 56 – col. 6, ln. 14). As such, M5 and M6 cause switching of inverters 33 and 34 to be delayed by holding the differential output V_{out-} from switching until V_{in+} is nearly V_{DD}. *Dai* does not expressly teach that M5 and M6 are a synchronized oscillator or operate as a synchronized oscillator. Furthermore, the Examiner has offered no support that M5 and M6 inherently teach a synchronized oscillator. The Examiner merely identifies specific components in Appellant's disclosure and declares that *Dai*'s memory element must operate the same. However, the Examiner ignores the actual connections of the components and supporting elements. The Examiner simply identifies particular components from the reference, construes them in a specific manner required by Appellants' claimed invention, and then states that the cited reference anticipates. *Dai* does not teach, expressly or inherently, a synchronized oscillator, since the memory element operates to maintain a constant output rather than an oscillating output.

Claims 2, 25-29 and 34-36

In the Examiner's Answer, the Examiner restates verbatim his arguments made in the August 5, 2008 Office Action with respect to these claims. Since the Examiner offers no new arguments for his position, the Applicant reiterates that the arguments discussed in the Appeal Brief still stand.

REQUESTED RELIEF

The Board is respectfully requested to reverse the outstanding rejections and return this application to the Examiner for allowance.

Respectfully submitted,

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